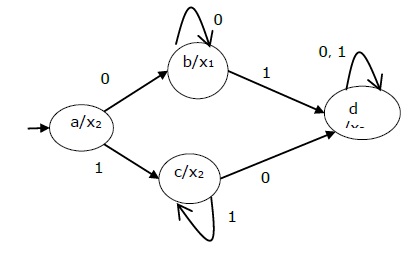
**LAB EXPERIMENT 11**

**Aim:** To design a sequence detector FSM in Xilinx software using Verilog programming. Design a sequence detector that detects a sequence of 1001. It is Moore type FSM.

**Theory:**

1. Moore Machine: Moore machine is an FSM whose outputs depend on only the present state.

FSM Diagram:



**Verilog Code of the Program and Outputs:**

1. **Verilog Code of the Program**

module moore\_062(

    input clk,

    input rst,

    input inp,

    output reg out

    );

reg [2:0] state;

always@(posedge clk or posedge rst)

begin

if(rst)

state<= 3'b000;

else

begin

case(state)

3'b000:begin

      if(inp)

state<=3'b001;

else

state<= 3'b000;

end

3'b001:begin

      if(inp)

state<=3'b001;

else

state<= 3'b010;

end

3'b010:begin

      if(inp)

state<=3'b001;

else

state<= 3'b011;

end

3'b011:begin

      if(inp)

state<=3'b100;

else

state<= 3'b000;

end

3'b100:begin

      if(inp)

state<=3'b001;

else

state<= 3'b010;

end

endcase

end

end

always@(posedge clk or posedge rst)

begin

if(rst)

out<=1'b0;

else if (state==3'b100)

out<=1'b1;

else

out<= 1'b0;

end

endmodule

1. **Screenshots of the Program:**

A picture containing text, screenshot, indoor

Description automatically generated

Graphical user interface

Description automatically generated

1. **RTL Schematic:**

A picture containing text, indoor, monitor, screenshot

Description automatically generated

Graphical user interface

Description automatically generated

**Conclusion:** From this experiment we have studies how to make a detector using Moore Machine. We also learnt how to put delays and check our output on Xilinx ISIM simulator.